MULTIMEDIA UNIVERSITY

STUDENT ID NO

Table Number	

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2016/2017

TMA1271 – INTRODUCTION TO MACHINE ARCHITECTURE

(All sections / Groups)

30 May 2017
2.30 pm – 4.30 pm
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 12 pages including cover page with 5 Questions only.

2. Attempt **ALL** the **FIVE** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in this booklet.

QUESTION 1

a) The John von Neumann architecture has been the basis for virtually all computer designs since the first generation. List and briefly explain the three design key concepts. [3 marks]

b) Draw the John von Neumann architecture. [2 marks]

c) A computer is a data processing machine which operates automatically under the control of a list of instructions stored in its main memory. List and briefly explain the **FOUR** basic functions of computer. [4 marks]

Continued ...

d) I/O and Memory may interrupt normal sequence of processing of the processor. List and briefly explain **THREE** most common classes of interrupts.

[3 marks]

QUESTION 2

In an Intel 8085 microprocessor, assume the following values are contained in the system's microprocessor's registers.

Register A (Accumulator)	contains 22_H
Register B	contains 11_H
Register C	contains 44_H
Register H	contains 77_H

The 8085 assembly language instructions in the program below are being executed in a single step mode.

```
ADD   B
MOV   C, A
MVI   H, 99H
```

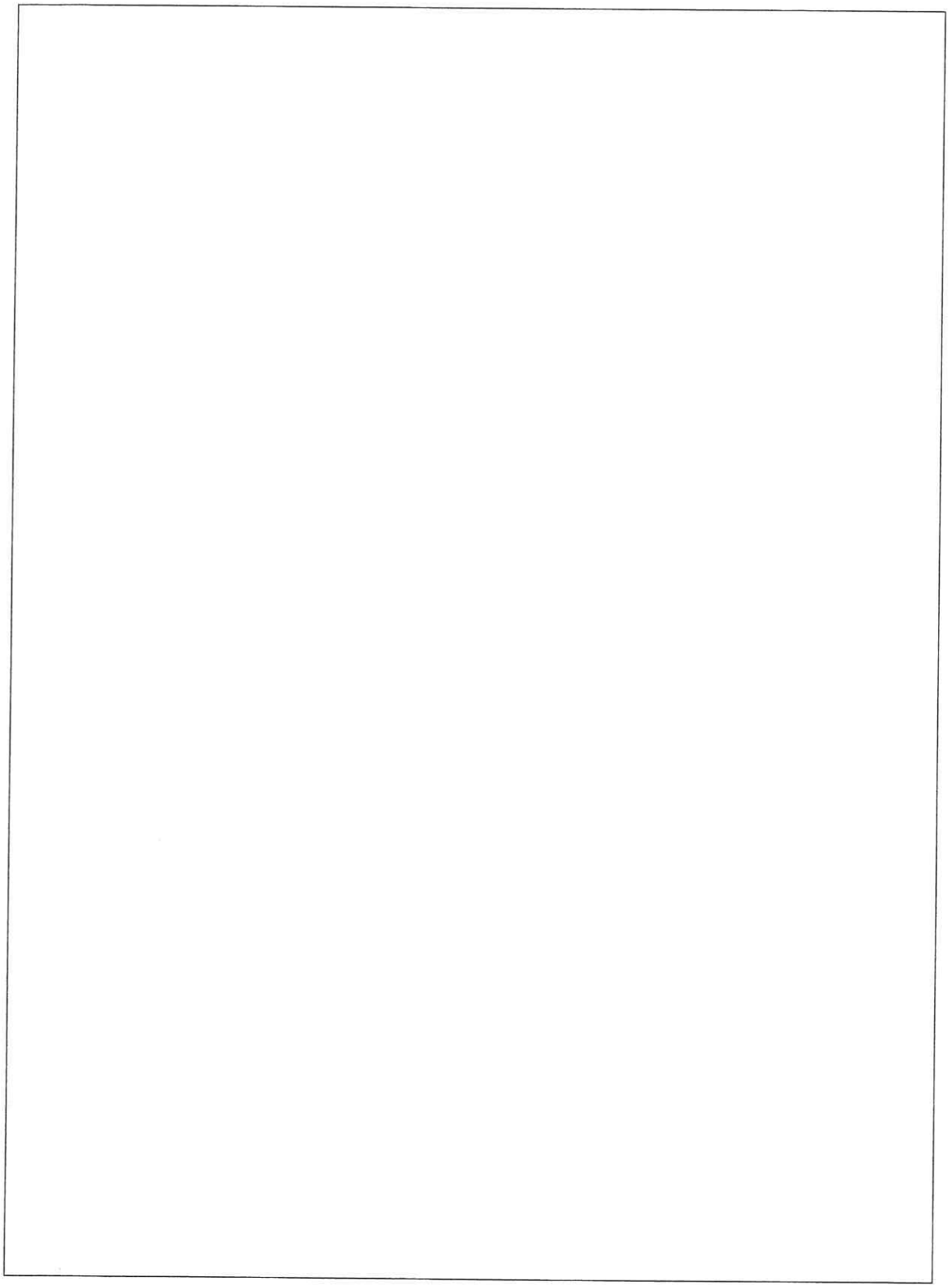
a) Based on the attached instructions and corresponding hexadecimal codes table (pages 11 and 12), provide the related hexadecimal value and related address mode for each instruction

[2 marks for each instruction, total 6 marks]

b) Assuming all the flag bits in flag register and microprocessor's registers are clear (reset) initially. State the contents of all four registers and status of the five flags after execution of each step.

[2 marks for each instruction, total 6 marks]

Continued ...



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QUESTION 3

a) Assume that an **8-bit two's complement** scheme is used for representing integers in a hypothetical machine.

i. Represent the following decimal numbers in binary using the machine in **8-bit two's complement format**.

1) $W = 22_{10}$
2) $X = -34_{10}$
3) $Z = 120_{103}$ [3 marks]

ii. Perform the following arithmetic operations in binary using this machine and identify if overflow occurs.

1) W + X
2) W+ Z [3 marks]

Continued ...

b) Assume there is a **five-stage** instruction pipeline - Fetch (F), Decode (D), Fetch Operand (FO), Execute (E) and Write (W) running in a microprocessor. Assume that each stage requires one time unit and no branch instruction is involved.

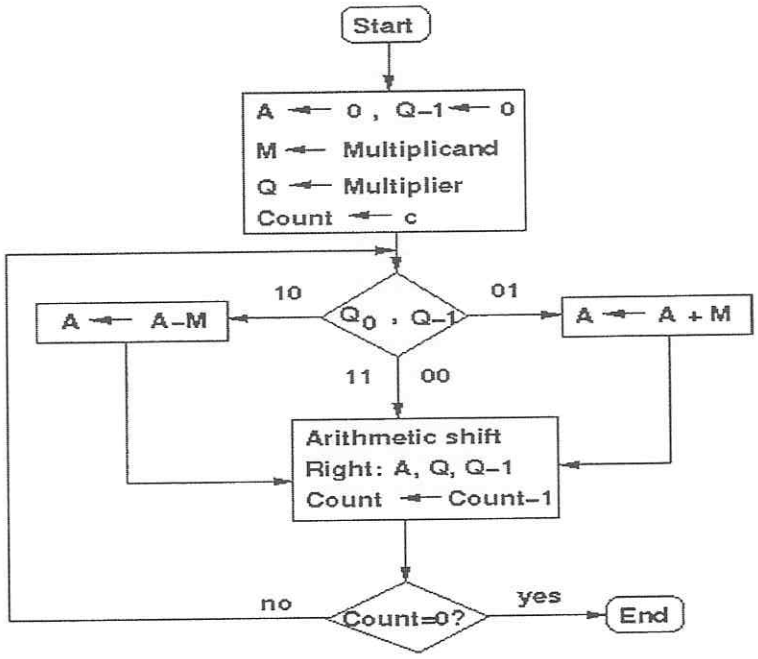
i. Draw the timing diagram for **FOUR** instructions.
ii. Based on the answer in (i), how many time units are needed to complete these four instructions with pipelining?
iii. By using formula, calculate the total time required to execute **FOUR** instructions without pipelining.
iv. Calculate the speedup factor for the same number of instructions.

[6 marks]

Continued ...

QUESTION 4

a) The flowchart for Booth's Algorithm is given below:



i) By applying the provided flowchart, perform multiplication by showing all the steps between the following 4-bit two's complement binary numbers, with multiplicand = 0111_2 ($+7_{10}$) and multiplier = 1101_2 (-3_{10}).

[5 marks]

ii) Convert the final product obtained from i) to decimal value.

[1 mark]

Continued ...

b) Write a program to evaluate the arithmetic expression W = (R - S) * T, using one address instructions, two address instructions and three address instructions. The instructions available for use are as follows:

One address	Two address	Three address
LOAD X	MOVE X ,Y	
STORE X	ADD X, Y	ADD X,Y,Z
ADD X	SUB X, Y	SUB X,Y,Z
SUB X	MUL X ,Y	MUL X,Y, Z
MUL X		

[6 marks]

One Instructions	Two Instructions	Three Instructions

Continued ...

QUESTION 5

a) In a general purpose computer system, the CPU, the main memory and the cache may be interconnected via system bus. However, I/O devices (e.g. hard disk, network interfaces) may only be connected to the system bus through an I/O controller. State any THREE reasons on why the I/O devices are not connected directly to the system bus.

[3 marks]

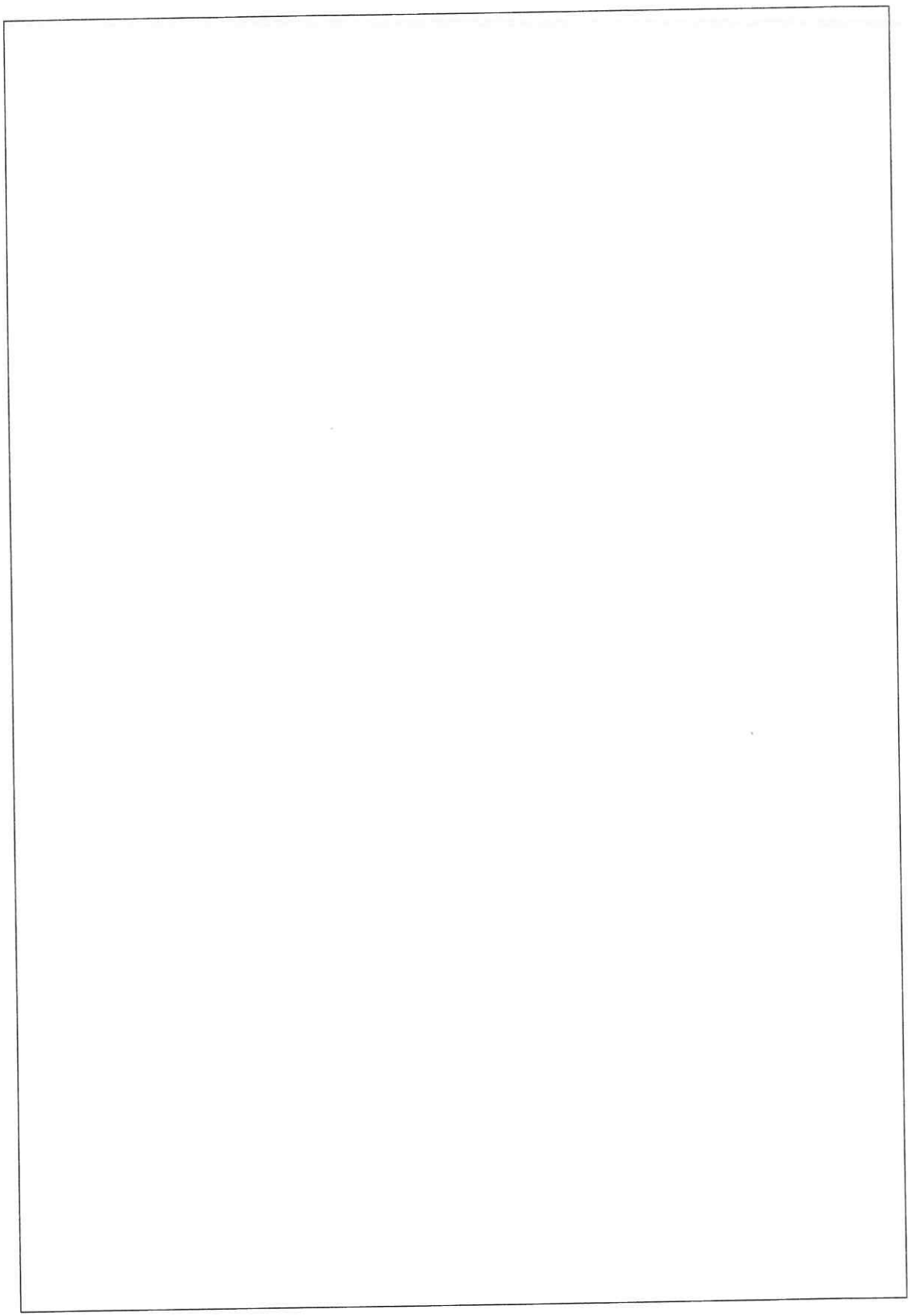
b) State the major difference between pipelining, superscalar organization and simultaneous multi-threading.

[3 marks]

c) Express the given negative decimal number (-123) in IEEE 754 standard, 32-bit single precision format.

[6 marks]

Continued ...



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Hex	Mnemonic	Hex	Mnemonic	Hex	Mnemonic	Hex	Mnemonic
CE	ACI 8-Bit	3F	CMC	2B	DCX H	01	LXI B,16-Bit
8F	ADC A	BF	CMP A	3B	DCX SP	11	LXI D,16-Bit
88	ADC B	B8	CMP B	F3	DI	21	LXI H,16-Bit
89	ADC C	B9	CMP C	FB	EI	31	LXI SP,16-Bit
8A	ADC D	BA	CMP D	76	HLT	7F	MOV A,A
8B	ADC E	BB	CMP E	DB	IN 8-Bit	78	MOV A,B
8C	ADC H	BC	CMP H	3C	INR A	79	MOV A,C
8D	ADC L	BD	CMP L	04	INR B	7A	MOV A,D
8E	ADC M	BE	CMP M	0C	INR C	7B	MOV A,E
87	ADD A	D4	CNC 16-Bit	14	INR D	7C	MOV A,H
80	ADD B	C4	CNZ 16-Bit	1C	INR E	7D	MOV A,L
81	ADD C	F4	CP 16-Bit	24	INR H	7E	MOV A,M
82	ADD D	EC	CPE 16-Bit	2C	INR L	47	MOV B,A
83	ADD E	FE	CPI 8-Bit	34	INR M	40	MOV B,B
84	ADD H	E4	CPO 16-Bit	03	INX B	41	MOV B,C
85	ADD L	CC	CZ 16-Bit	13	INX D	42	MOV B,D
86	ADD M	27	DAA	23	INX H	43	MOV B,E
C6	ADI 8-Bit	09	DAD B	33	INX SP	44	MOV B,H
A7	ANA A	19	DAD D	DA	JC 16-Bit	45	MOV B,L
A0	ANA B	29	DAD H	FA	JM 16-Bit	46	MOV B,M
A1	ANA C	39	DAD SP	C3	JMP 16-Bit	4F	MOV C,A
A2	ANA D	3D	DCR A	D2	JNC 16-Bit	48	MOV C,B
A3	ANA E	05	DCR B	C2	JNZ 16-Bit	49	MOV C,C
A4	ANA H	0D	DCR C	F2	JP 16-Bit	4A	MOV C,D
A5	ANA L	15	DCR D	EA	JPE 16-Bit	4B	MOV C,E
A6	ANA M	1D	DCR E	E2	JPO 16-Bit	4C	MOV C,H
E6	ANI 8-Bit	25	DCR H	CA	JZ 16-Bit	4D	MOV C,L
CD	CALL 16-Bit	2D	DCR L	3A	LDA 16-Bit	4E	MOV C,M
DC	CC 16-Bit	35	DCR M	0A	LDAX B	57	MOV D,A
FC	CM 16-Bit	0B	DCX B	1A	LDAX D	50	MOV D,B
2F	CMA	1B	DCX D	2A	LHLD 16-Bit	51	MOV D,C

Continued ...

Hex	Mnemonic	Hex	Mnemonic	Hex	Mnemonic	Hex	Mnemonic
52	MOV D,D	71	MOV M,C	E5	PUSH H	9E	SBB M
53	MOV D,E	72	MOV M,D	F5	PUSH PSW	DE	SBI 8-Bit
54	MOV D,H	73	MOV M,E	17	RAL	22	SHLD, 16-Bit
55	MOV D,L	74	MOV M,H	1F	RAR	30	SIM
56	MOV D,M	75	MOV M,L	D8	RC	F9	SPHL
5F	MOV E,A	3E	MVI A, 8-Bit	C9	RET	32	STA 16-Bit
58	MOV E,B	06	MVI B, 8-Bit	20	RIM	02	STAX B
59	MOV E,C	0E	MVI C, 8-Bit	07	RLC	12	STAX D
5A	MOV E,D	16	MVI D, 8-Bit	F8	RM	37	STC
5B	MOV E,E	1E	MVI E, 8-Bit	D0	RNC	97	SUB A
5C	MOV E,H	26	MVI H, 8-Bit	C0	RNZ	90	SUB B
5D	MOV E,L	2E	MVI L, 8-Bit	F0	RP	91	SUB C
5E	MOV E,M	36	MVI M, 8-Bit	E8	RPE	92	SUB D
67	MOV H,A	00	NOP	E0	RPO	93	SUB E
60	MOV H,B	B7	ORA A	0F	RRC	94	SUB H
61	MOV H,C	B0	ORA B	C7	RST 0	95	SUB L
62	MOV H,D	B1	ORA C	CF	RST 1	96	SUB M
63	MOV H,E	B2	ORA D	D7	RST 2	D6	SUI 8-Bit
64	MOV H,H	B3	ORA E	DF	RST 3	EB	XCHG
65	MOV H,L	B4	ORA H	E7	RST 4	AF	XRA A
66	MOV H,M	B5	ORA L	EF	RST 5	A8	XRA B
6F	MOV L,A	B6	ORA M	F7	RST 6	A9	XRA C
68	MOV L,B	F6	ORI 8-Bit	FF	RST 7	AA	XRA D
69	MOV L,C	D3	OUT 8-Bit	C8	RZ	AB	XRA E
6A	MOV L,D	E9	PCHL	9F	SBB A	AC	XRA H
6B	MOV L,E	C1	POP B	98	SBB B	AD	XRA L
6C	MOV L,H	D1	POP D	99	SBB C	AE	XRA M
6D	MOV L,L	E1	POP H	9A	SBB D	EE	XRI 8-Bit
6E	MOV L,M	F1	POP PSW	9B	SBB E	E3	XTHL
77	MOV M,A	C5	PUSH B	9C	SBB H		
70	MOV M,B	D5	PUSH D	9D	SBB L		

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